WHAT IS CLAIMED:

1. A known good integrated circuit having device optional solder ball array or wire bond connections:

solder ball array connections on an integrated circuit device surface;

an array of wire bond connections electrically connected to the solder ball array connections;

wherein known good integrated circuit device testing is completed prior to mounting the integrated circuit device on an end use device by connecting a test device by wire bond connections or by solder ball connections; and

wherein when either the wire bond connections are used or the solder ball connections are used for known good integrated circuit device testing, the other is available for connection to an end use device.

2. The known good integrated circuit device in accordance with claim 1, wherein when either the wire bond pad or the stress tolerant solder ball connections is used to form a contact with the test device, the other is not affected by a known good die (KGD) test.

3. The known good integrated circuit device in accordance with claim 1, wherein the wire bond pad connections and the solder ball array contacts are on the same side of the integrated circuit.

4. The known good integrated circuit device in accordance with claim 1, wherein the solder ball array connections and the wire bond pads are on the substantially the same level of the integrated

circuit so that either may provide contact with an end use device.

5. The known good integrated circuit device in accordance with claim 1, wherein the solder ball array or wire bond pads used for testing are not removed from the integrated circuit after testing

6. The known good integrated circuit device in accordance with claim 1, wherein connections to the test device are metallurgical connections.

7. The known good integrated circuit device in accordance with claim 1, wherein the solder ball array connections are controlled collapse chip connections.

8. The known good integrated circuit device in accordance with claim 1, wherein the solder ball array is a stress tolerant solder ball array.

9. The known good integrated circuit device in accordance with claim 1, wherein the integrated circuit device is a die.

10. The known good integrated circuit device in accordance with claim 1 wherein the integrated circuit device is connected to an end use device.

11. A method of making a known good integrated circuit device for solder ball array connection to an end use device comprising the steps of:

constructing an integrated circuit device having wire bond pads, and a solder ball array, wherein the solder ball array is connected to the wire bond pads by connections on the integrated circuit;

after constructing the integrated circuit device connecting

the integrated circuit device to a test device with the wire bond pads; and

testing the integrated circuit device.

12. The method in accordance with claim 11, further comprising leaving the solder ball array contacts in pristine condition.

13. The method in accordance with claim 11, further comprising heavily leading the solder ball array.

14. The method in accordance with claim 11, wherein said testing is a cyclic temperature test.

15. A method in accordance with claim 11, further comprising the step of placing the solder ball array connections and the wire bond pads on the same substantially planar surface.

16. A method in accordance with claim 11, further comprising metallurgically bonding the wire bond pads to the test device.

17. A method in accordance with claim 11, wherein said integrated circuit device is a die.

18. The method in accordance with claim 11, further comprising constructing stress tolerant solder ball connections.

19. The method in accordance with claim 11, further comprising connecting the integrated circuit device to an end use device after testing.

20. A method of making a known good integrated circuit device having wire bond connections for connection to an end use device comprising the steps of:

forming wire bond pads on the integrated circuit device;

forming a stress tolerant solder ball array on the integrated

circuit device;

connecting the stress tolerant solder ball array to the wire bond pads; and

using the stress tolerant solder ball array to metallurgically connect the integrated circuit device to a known good integrated circuit test device; and

testing the integrated circuit.

21. The method in accordance with claim 20, further comprising leaving the wire bond pad connections in pristine condition.

22. The method in accordance with claim 20, further comprising forming the stress tolerant solder ball array contacts using heavily leaded soldered balls.

23. The method in accordance with claim 20, wherein said testing is a cyclic temperature test.

24. A method in accordance with claim 20, further comprising removing the integrated circuit device from the test device by reheating balls of the stress tolerant solder ball array.

25. A method in accordance with claim 24, further comprising a step of leaving a taffy pull configuration when the solder balls are drawn away.

26. A method in accordance with claim 24, further comprising a step of causing stress tolerant solder ball array balls to sheer in the middle on the reheating for removal.

27. A method in accordance with claim 20, wherein said integrated circuit device is a die.

28. The method in accordance with claim 20, further comprising

connecting the integrated circuit device to an end use device after testing.

29. A method of testing a known good integrated circuit device having stress tolerant solder ball array connections for connecting to an end use device comprising the steps of:

constructing on a surface of the integrated circuit device a stress tolerant solder ball array of connections;

constructing on a surface of the integrated circuit wire bond pads which are connected to the stress tolerant solder ball array of connections;

testing said die by forming metallic connections between said wire bond pads and a test device; and

removing said metallic connections from said wire bond pads after testing said die.

30. A method in accordance with claim 29, further comprising the step of placing the stress tolerant solder ball array connections and the wire bond pads on the same substantially planar surface.

31. A method in accordance with claim 29, wherein said testing is cyclic temperature burn-in testing.

32. A method in accordance with claim 29, wherein the testing is at the integrated circuit level.

33. A method in accordance with claim 29, further comprising bonding the wire bond pads metallurgically to a test device.

34. The method in accordance with claim 29, further comprising leaving the stress tolerant solder ball array contacts in pristine condition.

35. The method in accordance with claim 29, further comprising heavily leading the stress tolerant solder ball array.

36. A method of testing an integrated circuit having wire bond connections for connecting to an end use device comprising the steps of:

constructing on a surface of the integrated circuit a stress tolerant solder ball array of connections;

constructing on a surface of the integrated circuit device wire bond pads which are connected to the stress tolerant solder ball array connections;

testing said integrated circuit device by forming metallic connections between the stress tolerant solder ball array connections and a test device; and

removing said metallic connections after testing said integrated circuit.

37. A method of testing a known good integrated circuit having wire bond connections for connecting to a an end use device in accordance with claim 35, further comprising removing by reheating solder balls of the stress tolerant solder ball array which are connected to the test device.

38. A method of testing a known good integrated circuit having wire bond connections for connecting to a to an end use device in accordance with claim 36, further comprising a step of leaving a taffay pull configuration when the solder is drawn away.

39. A method of testing a known good integrated circuit having wire bond connections for connecting to an end use device in

accordance with claim 35, further comprising the step of forming a stress tolerant solder ball array balls which are heavily leaded.

40. A method of testing a known good integrated circuit having wire bond connections for connecting to an end use device in accordance with claim 35, further comprising a step of causing stress tolerant solder ball array balls to sheer in the middle after reheating.

41. A method of testing a known good integrated circuit having wire bond connections for connecting to an end use device, in accordance with claim 35, further comprising forming metallurgical connections between the stress tolerant solder ball array and the test substrate.

42. The method in accordance with claim 35, further comprising leaving the wire bond pad connections in pristine condition.

43. The method in accordance with claim 35, wherein said testing is a cyclic temperature burn-in test.